a pulse generator responsive to the received input train of pulses produced at the output of the receiver for producing first pulses in response to [the] leading edges of the received input train of pulses and second pulses in response to [the] trailing edges of the received input train of pulses, the leading [edge] edges of the first [pulse] pulses having the same edge type as the leading [edge] edges of the second [pulse] pulses;

a logic network for combining the first pulses and the second pulses into a composite input signal comprising the first and second pulses with the leading [edge] edges of the first [pulse] pulses maintaining the same edge type;

a variable delay line fed by the composite input signal for producing a composite output train of pulses comprising both the first train of pulses and the second train of pulses after a [selected] time delay [provided by the delay line; and

wherein the delay-locked-loop is responsive to] selected in accordance with the first pulses, second pulses and one of the first train of pulses and the second train of pulses in the composite output train of pulses [for selecting the time delay of the variable delay line to produce such composite output train of pulses with a predetermined phase relationship with the input train of pulses].

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4. (Amended) The circuit recited in claim 3 wherein the phase comparator includes a first input fed by pulses in the output train of pulses and a second input fed by pulses in the received train of input pulses and

wherein the delay-locked-loop includes:

a gate fed by the output train of pulses and a gating signal; and

a gate pulse generator responsive to one of the first and second pulses for producing the gating signal during the first pulse to enable the output train of pulses to pass through [such] said gate to the phase comparator and to inhibit the output train of pulses from passing through the gate to the phase comparator during the second pulse.

5. (Amended) The circuit recited in claim 2 wherein the phase comparator includes a first input fed by pulses in the output train of pulses and a second input fed by pulses in the received train of input pulses and

wherein the delay-locked-loop includes:

a gate fed by the output train of pulses and a gating signal; and

a gate pulse generator responsive to one of the first and second pulses for producing the gating signal during the first pulse to enable the output train of pulses to pass through [such] said gate to the phase comparator and to inhibit the output train of pulses from passing through the gate to the phase comparator during the second pulse.

6. (Amended) A circuit, comprising:

a receiver for receiving an input train of pulses;

a pulse generating circuit coupled to an output of the receiver for producing a first pulse in response to a leading edge of each one of the pulses in the input train of pulses and a second pulse in response to [the] a trailing edge of each one of the pulses in the input train of pulses, the leading edges of the first and second pulses having the same edge type;

a variable delay line responsive to the first and second pulses for producing corresponding first and second output pulses, each one of [such] said first and second output pulses being produced in response to the corresponding one of the first and second pulses after a time delay selected in accordance with a control signal fed to the variable delay line;

a phase comparator having a first input fed by one of the first and second pulses and a second input fed by the corresponding one of the first and second output pulses, for producing the control signal, [such] said control signal selecting the time delay for the variable delay line to produce the output pulses with the leading edges timed coincident with leading edges of the pulses in the input train of pulses.

8. (Amended) The circuit recited in claim 7 wherein the phase comparator includes a first input fed by pulses in the output train of pulses and a second input fed by pulses in the received train of input pulses and including:

a gate fed by the output train of pulses and a gating signal; and

a gate pulse generator responsive to one of the first and second pulses for producing the gating signal during the first pulse to enable the output train of pulses to pass through [such] said gate to the phase comparator and to inhibit the output train of pulses from passing through the gate to the phase comparator during the second pulse.

9. (Amended) The circuit recited in claim 6 wherein the phase comparator includes a first input fed by pulses in the output train of pulses and a second input fed by pulses in the received train of input pulses and including:

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a gate fed by the output train of pulses and a gating signal; and

a gate pulse generator responsive to one of the first and second pulses for producing the gating signal during the first pulse to enable the output train of pulses to pass through [such] said gate to the phase comparator and to inhibit the output train of pulses from passing through the gate to the phase comparator during the second pulse.

10. (Amended) A circuit, comprising:

a receiver for receiving an input train of pulses, [such] said train of pulses having a period, T, [such] said receiver providing a first time delay, Δ_1 to the pulses in the input train of pulses;

a pulse generating circuit coupled to an output of the receiver for producing a first pulse in response to a leading edge of each one of the pulses in the input train of pulses and a second pulse in response to a trailing edge of each one of the pulses in the input train of pulses, the leading edges of the first and second pulses having the same edge type, [such] said pulse generating circuit producing the first pulses and the second pulses with a second time delay Δ_2 after the leading edge of pulses in the input train of pulses;

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a logic network for combining the first pulses and the second pulses into a composite input signal comprising the first and second pulses with the leading edge of the first pulse maintaining the same edge type, [such] said logic network providing a third time delay Δ_3 to the first and second pulses;

a variable delay line responsive to the first and second pulses for producing corresponding first and second output pulses, each one of [such] said first and second output pulses being produced in response to the corresponding one of the first and second pulses after a time delay Δ_L selected in accordance with a control signal fed to the variable delay line;

a delay network fed by the output train of pulses [such] said delay network providing a fourth time delay Δ_4 related to $\Delta_1+\Delta_2$;

a phase comparator having a first input fed by one of the first and second pulses and a second input coupled to an output of the delay network, for producing the control signal, [such] said control signal selecting the time delay Δ_L equal to $nT-(\Delta_1+\Delta_2+\Delta_3)$, where n is an integer to produce the output pulses having leading edges timed coincident with leading edges of the pulses in the input train of pulses.

11. (Amended) The circuit recited in claim 10 wherein the phase comparator includes a first input fed by pulses in the output train of pulses and a second input fed by pulses in the received train of input pulses and including:

a gate fed by the output train of pulses and a gating signal; and

a gate pulse generator responsive to one of the first and second pulses for producing the gating signal during the first pulse to enable the output train of pulses to pass through [such] said gate to the phase comparator and to inhibit the output train of pulses from passing through the gate to the phase comparator during the second pulse.

12. (Amended) A method for generating a train of output pulses having a predetermined phase relationship with a train of input pulses, comprising:

passing the input train of pulses through a receiver;